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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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David Alan Eward

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01/26/2005

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EXAMINER

VO, TED T

ART UNIT

PAPER NUMBER

2122

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/411,792

Applicant(s)

EWARD ET AL.

Examiner

Ted T. Vo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-64 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-64 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is in response to the claimed amendment filed under Request for Continued Examination on 09/22/2004. Accordingly, this action is non-final.

Claims 1, 21-22, and 42 are amended.

Claims 1-64 are pending in the application.

Response to Arguments

2. Applicants' arguments to the newly added limitations have been fully considered.

For example, with regard to the buffer captures debug information from the memory, Applicants argue that instruction address is an operand value, not the operand address.

Examiner responds: In regards to the example of add instruction such as add 5, 7, it should be noted that it is known in the art the term value 5 or the value 7 is the operand value. However, referring to the buffer 70, it does not indicate an operand value like value 5 or value 7 only, it stores and traces the contents of memory including, "address information", "target address value", "instruction address", "Program Counter Breakpoint value", etc for debug purposes (See Circello).

As per Applicants' argument, *"The operand associated with branch or jump instruction is the location in the memory to which execution is to branch or jump. Thus, in the case of a branch or jump instruction the operand value is a memory address. This address represents the value of operand on which the branch is to be performed. This address does not represent an address in memory at which an operand value is stored"* (Remarks: page 13, lines 7-11):

First of all, the reference (Circello) does not only teach a particularly thing like capture jump or branch address, it discloses tracing as well. The jump or branch address in each of these instructions corresponds to a program counter value/instruction address that points to a new instruction where an external development looks at to examine. It is known that tracing traces the content of a memory.

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Without the instruction address/program counter value, the trace cannot find the content of an instruction. In this particular thing, the "instruction address" of the branch/jump corresponds with a value in the program instruction address, i.e. the address of a new location like any location shown in a table within column 22, lines 27-35. Thus, "instruction address" also represents *an address value (instruction address)* in this reference's program counter to indicate a location of the stored instruction in the memory where branch control reaches up to.

It should be noted that, the term "operand address" is not defined clearly. With the interpretation in light of the specification, "operand address" is interpreted as instruction address or program counter value because only the instruction address or the program counter does the indication of memory location. Within one of embodiments, each of the reference's terms, "target address value", "address information", and "program counter breakpoint value", etc., becomes the address value in this reference's program counter that points to a location in memory to help the debug circuit to examine the instructions. It is known that a conventional processor memory includes a program counter wherein the counter increments or is set to an instruction code in memory. The "Instruction Address" and "Instructions" as used in the table within column 22, express such a convention. The terminology, "program counter value" or of "instruction address", or even "operand address", the limitation in the Claims, each expresses the functionality of a value of a program counter to which a location of a stored information in the memory is resided. For example, in the table, the Instruction address, "00001316" tells the processor where the location of instruction (operands) `movq; #1,d0` is. Within another embodiment, the reference discloses such an indication of a memory location at which an operand value is stored, "*The DDATA signal (Examiner note: Data coming out from Debug Module of FIG. 2) also provides captured instruction address program flow changes to allow an external development system to trace an exact program flow without requiring an externally visible address bus or an externally visible data bus. Note that the information displayed on the DDATA signal is synchronized with the status information on the PST signals*" (Column 15, lines 12-18: see Col. 14, lines 65-67 and Col. 15, lines 1-23). It shows that the buffer within circuit 14 captures the contents of memory including "Instruction Address" and "Instructions"

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as of the table within column 22. It should be noted that if only the operand values are captures, the external development couldn't trace the flow change.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-64 are rejected under 35 U.S.C. 102(b) as being anticipated by Circello et al. (US No. 5,737,516), submitted by applicants.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 1:

Circello teaches, "*At least one processor* (FIG. 1, figure feature core 9);

a debug circuit (FIG. 1, all circuitries connecting to figure feature core 9);

a system bus coupling the processor and debug circuit (See FIG. 1, S-BUS, M-BUS, or K-BUS etc. (*system bus*); and K-BUS, CPST, BUS REQUEST, BUS GRANT, STALL, BREAKPOINT CONTROL (*communication link*)); and

a communication link coupling the processor and debug circuit (see figure 2, all connections/bus between core 9 and the debug module 10), *where the processor is configured to transmit to the debug through the communication link a plurality of bit values each representing a state of an operation* (see Column 3, lines 54-59, having means for *transmit, operand address, representing a state*) *in the processor including at least an operand address that indicates a memory location at which an operand value is stored* (See column 20, lines 27-61, particularly, *take branch*, value on the CPST, *capture an*

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instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline (operand address; See Col. 14, lines 65-67 and Col. 15, lines 1-23).

As per Claim 2: Circello shows KCONTROL and K-BUS that relates together in debugging, (column 4, lines 55-67), and discusses a pipeline operation that produces outputs to KADDR and KDATA of K-BUS (see column 6, lines 5-25).

As per Claim 3: In coupled with K-BUS, Circello discusses a register that stores program counter breakpoint (see column 9, lines 49-61).

As per Claim 4: Being inherent from debug mode operation (column 12, lines 35-39). Circello teaches that the counter program breakpoint defines a region in a local address space (see column 13, lines 37-50) belonged to a data processing system (FIG. 1) might be used to trigger breakpoint function. It further provides pipelines accessibility to cause a step instruction execution (see started column 19, line 64 to column 20, line 61).

As per Claim 5: Circello teaches inherently the limitation in discussing the trigger response (see column 29, lines 24-40).

As per Claim 6: Regarding limitation, "a first instruction past a branch instruction", Circello teaches inherently the limitation in using the value, %0101 of the PST signal (see column 15, lines 46-50).

As per Claim 7: Circello teaches inherently the limitation in using the values of the PST signal (see column 15, lines 46-50) for indicating branch or return instructions, where the PST receives information from K-BUS.

As per Claim 8: Circello discloses real-time tracing that provides a unique trace function (see column 22, lines 14-16).

As per Claim 9: Circello discloses a PST that receives information from K-BUS to provide bit information to reflect an execution status of the CPU (see column 15, lines 10-2).

As per Claim 10: Circello discloses the PST that receives information from K-BUS to assert some of bit values for exception processing (see FIG. 10).

As per Claim 11: Circello discloses the mechanism in the figure 2 that is configured to transmit debug information to the debug module via K-Bus and control links connected to the core 9.

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As per Claim 12: Circello discloses the PST that receives information from K-BUS to assert bit values (FIG. 10). Some of these bit values indicate executions of instructions.

As per Claim 13: Circello discloses the PST that receives information from K-BUS to assert bit values (FIG. 10). Some of these bit values indicate identifier information of executions. For example, one of bit values indicates that a branch is taken.

As per Claim 14: Circello provides debugging which is capable of performing exception/interrupt handling (FIG. 10, or column, 8, lines 35-41).

As per Claim 15: Claims limitation is inherent in bits values. For example, the signal from K_BUS causes the control 60 to generate PST and DDATA. The table in columns 22-23 describes bit values of the DDATA, where these values are used by external development system to view the execution of instructions.

As per Claim 16: For a matching with a memory address access by the processor in response to an execution instruction is inherent in branching/jumping or exception/interrupt.

As per Claim 17: Being inherent in execution of single instruction step mode (column 11, lines 55-56) or the status that indicates, 'begin execution of an instruction' (FIG. 10).

As per Claim 18: Circello discloses the PST that receives information from K-BUS to assert bit values (FIG. 10). Some of these bit values indicate identifier information of executions. For example, one of bit values indicates that a branch is taken.

As per Claim 19: Being inherent in execution of tracing function (see column 22, lines 14-25) or the status that indicates, 'begin execution of an instruction' (FIG. 10).

As per Claim 20: FIG. 1 has means of a single integrated circuit.

As per Claim 21:

Circello discloses, "*At least one processor* (FIG. 1, figure feature core 9);

a debug circuit (FIG. 1, all circuitries connecting to figure feature core 9);

a system bus coupling the processor and debug circuit (See FIG. 1, S-BUS, M-BUS, or K-BUS etc (system bus)); and

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a communication link coupling the processor and debug circuit (See FIG. 1, K-BUS, CPST, BUS REQUEST, BUS GRANT, STALL, BREAKPOINT CONTROL (communication link), where the processor is configured to transmit to the debug through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of: and

an operand address that indicates a memory location at which an operand value is stored (See Col. 14, lines 65-67 and Col. 15, lines 1-23); and an operand value (See column 20, lines 27-61, particularly, take branch, value on the CPST, "capture an instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline": 'operand address and operand value');

where the processor is further configured to transmit to the debug circuit: a program counter value indicating the program counter of the processor at a writeback stage of a pipeline of the processor, a status indicating that a computer instruction is in the writeback stage is valid computer instruction (See, Column 20, lines 27-62, pipeline, instruction address of "Target". As the JMP instruction occupies the AGEX stage of the operand execution pipelines; see column 13, lines 37-64, Program Counter Breakpoint, data signal transferred via K-Bus 25..."); a status indicating that the computer instruction in the writeback stage is a first instruction past an execute branch instruction; a status indicating a type of executed branch instruction and process identifier information of an executed instruction (See started from column 12, line 15 to column 13, line 64, teaching of address space that defines a range started with a breakpoint location; and see DDATA bit definitions, the table in columns 22-23).

As per Claims 22, 42: The claims have the claimed functionality corresponding to the functionality of Claim 1. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 1.

As per Claims 23, 43: The claims have the claimed functionality corresponding to the functionality of Claim 2. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 2.

As per Claim 24: The claim has the claimed functionality corresponding to the functionality of Claim 3. Claim is rejected in the same reasons set forth in connecting to the rejection of Claim 3.

As per Claims 25, 44: The claims have the claimed functionality corresponding to the functionality of Claim 4. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 4.

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As per Claims 26, 45: The claims have the claimed functionality corresponding to the functionality of Claim 5. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 5.

As per Claims 27, 46: The claims have the claimed functionality corresponding to the functionality of Claim 6. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 6.

As per Claim 28, 47: The claims have the claimed functionality corresponding to the functionality of Claim 7. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 7.

As per Claim 29, 48: The claims have the claimed functionality corresponding to the functionality of Claim 8. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 8.

As per Claims 30, 49: The claims have the claimed functionality corresponding to the functionality of Claim 9. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 9.

As per Claims 31, 50: The claims have the claimed functionality corresponding to the functionality of Claim 10. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 10.

As per Claims 32, 51: The claims have the claimed functionality corresponding to the functionality of Claim 11. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 11.

As per Claims 33, 52: The claims have the claimed functionality corresponding to the functionality of Claim 12. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 12.

As per Claims 34, 53: The claims have the claimed functionality corresponding to the functionality of Claim 13. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 13.

As per Claims 35, 54: The claims have the claimed functionality corresponding to the functionality of Claim 14. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 14.

As per Claims 36, 55: The claims have the claimed functionality corresponding to the functionality of Claim 15. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 15.

As per Claims 37, 56: The claims have the claimed functionality corresponding to the functionality of Claim 16. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 16.

As per Claims 38, 57: The claims have the claimed functionality corresponding to the functionality of Claim 17. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 17.

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As per Claims 39, 58: The claims have the claimed functionality corresponding to the functionality of Claim 18. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 18.

As per Claims 40, 59: The claims have the claimed functionality corresponding to the functionality of Claim 19. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 19.

As per Claims 41, 60: The claims have the claimed functionality corresponding to the functionality of Claim 20. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 20.

As per Claim 61: Circello discloses the claim limitation (See column 20, lines 27-61, particularly, *take branch, value on the CPST, capture an instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline* (operand address and operand value); and see FIG.2, the K-BUS connected to the to the FIFO 70; and see Col. 14, lines 65-67 and Col. 15, lines 1-23).

As per Claim 62: Circello discloses the claim limitation (See column 20, lines 27-61, particularly, *take branch, value on the CPST, capture an instruction address Target at the conclusion of the IC cycle of an instruction fetch pipeline* (operand address and operand value); and see FIG.2, the K-BUS connected to the to the FIFO 70, and see Col. 14, lines 65-67 and Col. 15, lines 1-23);

As per Claims 63, 64: The claims have the claimed functionality corresponding to the functionality of Claim 62. Claims are rejected in the same reasons set forth in connecting to the rejection of Claim 62.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3694. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from

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either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Ted T. Vo', is positioned above the printed name.

Ted T. Vo
Patent Examiner
Art Unit 2122
January 21, 2004